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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,661	05/14/2001	Masahiro Tanaka	208546US2	6508
22850	7590 11/18/2004		EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET			DIAZ, JOSE R	
ALEXANDRIA, VA 22314		ART UNIT	PAPER NUMBER	
	,		2815	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary  Examiner  José R. Díaz  The MAILING DATE of this communication appears on the cover sheet with the correspondence address  Period for Reply  TANAKA, MASAHIRO  2815  2815  Period for Reply	<del>/-</del>					
José R. Díaz 2815  The MAILING DATE of this communication appears on the cover sheet with the correspondence address						
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A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on <u>23 August 2004</u> .						
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This action is non-final.						
Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1,2,4-6,16-19 and 27-42</u> is/are pending in the application.						
4a) Of the above claim(s) 6,19,31-34 and 39-42 is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1,2,4,5,16-18,27-30 and 35-38</u> is/are rejected.						
· ·	Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner.						
10) The drawing(s) filed on is/are: a) □ accepted or b) □ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a)⊠ All b)☐ Some * c)☐ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  Paper No(s)/Mail Date  Notice of Informal Patent Application (PTO-152)						
Paper No(s)/Mail Date 11/13/03;4/6/04;7/30/04  6) Other:  S. Patent and Trademark Office						

23, 2004 has been entered.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August

2. Newly submitted claims 31-34 and 39-42 directed to an invention that is

Election/Restrictions

independent or distinct from the invention originally claimed for the following reasons:

claims 31-34 and 39-42 are directed to the non elected Species II.

Since applicant has received an action on the merits for the originally presented

invention, this invention has been constructively elected by original presentation for

prosecution on the merits. Accordingly, claims 31-34 and 39-42 withdrawn from

consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and

MPEP § 821.03.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 1-2, 4-5, 16-18, 27-30 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuwahara (US Pat. No. 5,44,271) in view of Roman et al. (US Pat. No. 4,053,924).

Regarding claims 1, 4, 16, 27-30 and 35-38, Kuwahara teaches an IGBT semiconductor device comprising:

a first-conductivity-type semiconductor substrate (12) (see fig. 1);

a second-conductivity-type base region (13-1, 13-2) formed in one surface of the semiconductor substrate (see fig. 1);

a first-conductivity-type impurity region (14-1, 14-2, 14-3, 14-4) formed in the base region (see fig. 1);

a first electrode (17-1, 17-2) connected to the first-conductivity-type impurity region (see fig. 1);

a gate electrode (16-1) connected to the base region via an insulation film (15-1) (see fig. 1);

a second-conductivity-type impurity region (11) formed in another surface of the semiconductor substrate (see fig. 1);

a second-conductivity-type contact region (21) formed in the second-conductivity-type impurity region (see fig. 1) and having a thickness of not more than  $0.2~\mu m$  from the another surface of the semiconductor substrate (see col. 6, lines 38-40), the contact region (21) being thinner than the second-conductivity- type impurity region (11) (see

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fig. 1) and a peak of an impurity concentration (i.e.  $10^{18}$ - $10^{20}$  cm<sup>-3</sup>) of the second-conductivity-type contact region (21) being higher than that (i.e.  $10^{16}$ - $10^{18}$  cm<sup>-3</sup>) of the second-conductivity-type impurity region (11) (see col. 6, lines 32-33 and 38-39); and a second electrode (19) formed on the contact region (see fig. 1).

However, Kuwahara fails to teach the limitation about the second-conductivity-type impurity region having a thickness of more than 0.2  $\mu m$  and not more than 1.0  $\mu m$  from another surface of the semiconductor substrate.

Roman et al. teaches that it is very well known in the art to use a thin second-conductivity-type impurity region (34) of not more than 1.0  $\mu$ m thick (i.e. 50-200 Å thick. Please note that this thickness is taken from the interface formed between the second-conductivity-type impurity region 32 and the second-conductivity-type contact region 34) [see col. 10, lines 13-16 and 62-63]. Furthermore, Roman et al. teaches second-conductivity-type contact region (32) having a thickness of less than about 0.2  $\mu$ m (i.e. 300-800 Å) (see col. 10, lines 10-12).

With regards to the claimed limitation that the second-conductivity-type impurity region also has a thickness of more than 0.2  $\mu$ m, Roman et al., as stated before, provides a general teaching of using a thin second-conductivity-type impurity region (34) having, for example, a thickness of about 300-800 Å which is less than the claimed range of not more than 1.0  $\mu$ m. However, Roman et al. is silent with respect of a thickness of more than 0.2  $\mu$ m and not more than 1.0  $\mu$ m. It would have been obvious to one of ordinary skill in the art to include a thin second-conductivity-type impurity region of more than 0.2  $\mu$ m and not more than 1.0  $\mu$ m, since it has been held that where the

general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Huang*, 40 USPQ2d 1685,1688(Fed. Cir. 1996) citing *In re Aller*, 105 USPQ 233., 235 (CCPA 1955). The motivation for doing so is to provide a low forward turn-on voltage

Kuwahara and Roman et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a second-conductivity-type impurity region having a thickness of more than 0.2 μm and more than 1.0 μm. The motivation for doing so, as is taught by Roman et al., is to improve the forward and reverse recovery times of the junction without degrading the steady state reverse current characteristic (abstract). Therefore, it would have been obvious to combine Roman et al. with Kuwahara to obtain the invention of claims 1-2, 4-5, 16-18, 27-30 and 35-38.

Regarding claims 2 and 17, Kuwahara teaches the impurity layer is provided for carrier injection from the impurity layer to the semiconductor substrate, and the contact layer is provided for reducing a contact resistance between the first electrode and the impurity layer and not for carrier injection (see col. 7, lines 1-19).

Regarding claims 5 and 18, Kuwahara teaches that the second second-conductivity-type impurity region (11) is formed in the entire one surface of the semiconductor substrate (12) (see fig. 1).

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## Response to Arguments

5. Applicant's arguments with respect to claims 1-2, 4-5, 16-18, 27-30 and 35-38 have been considered but are moot in view of the new ground of rejection.

## Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Roggwiller (US Pat. No. 4,961,099) discloses shallow p-type regions (6) in a p-type layer (9) in figure 2; and Sakurai (US Pat. No. 5,200,632) discloses shallow p-type regions (1) in another p-type regions (12) in figure 1.

## Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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JRD 11/14/04

GEORGE ECKERT